# TFE4152 - Project: Design of Digital Camera

REPORT

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# 1 Abstract

One can argue that out of all the impressive inventions mankind has produced throughout the years, the camera is one of the most significant. Humans have always had a need to preserve and present the world around us through imagery, and the earliest paintings can be dated back thousands of years. When the first photograph was taken in the early 19th century it completely changed the way people would document events. As the quality and accessibility improved it became easier than ever to share and preserve parts of life. Today high quality digital images play a significant role in everyday life. As the world became increasingly more digitalized, so did the camera. Today everyone carries devices with a digital camera installed. This allows us to capture and immediately store the image digitally for it to be shared with people around the world.

In this article, the design of a simple four pixel black and white digital camera with adjustable exposure time will be discussed. Two aspects of the camera design will be discussed; the analog circuit responsible for capturing the photograph and the digital control which is tasked with toggling control signals at desired instances of time. The camera will not be implemented physically but the behaviour of both the analog circuit and digital control unit will be simulated using computer software. The analog circuit will be simulated using the analog electronic circuit simulator AIM-Spice. The digital control will be simulated using the hardware description language Verilog.

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# 2 Introduction

A flow chart of a digital camera is shown in Figure 2. Although the camera to be designed is digital there exists a need for an analog circuit to capture the light from the environment. When the user initiates the capturing of a photo this analog circuit takes light as its input and stores the amount of light each pixel "sees". In order for the photograph to be stored digitally the analog value representing the amount of light in each pixel has to be read out from the analog circuit, converted to a binary number and stored in memory. In order for the camera to know when to perform the different actions needed, a digital control unit governs when the different components are to perform their tasks. As previously mentioned the components of discussion will be the analog readout circuit and the digital control unit.

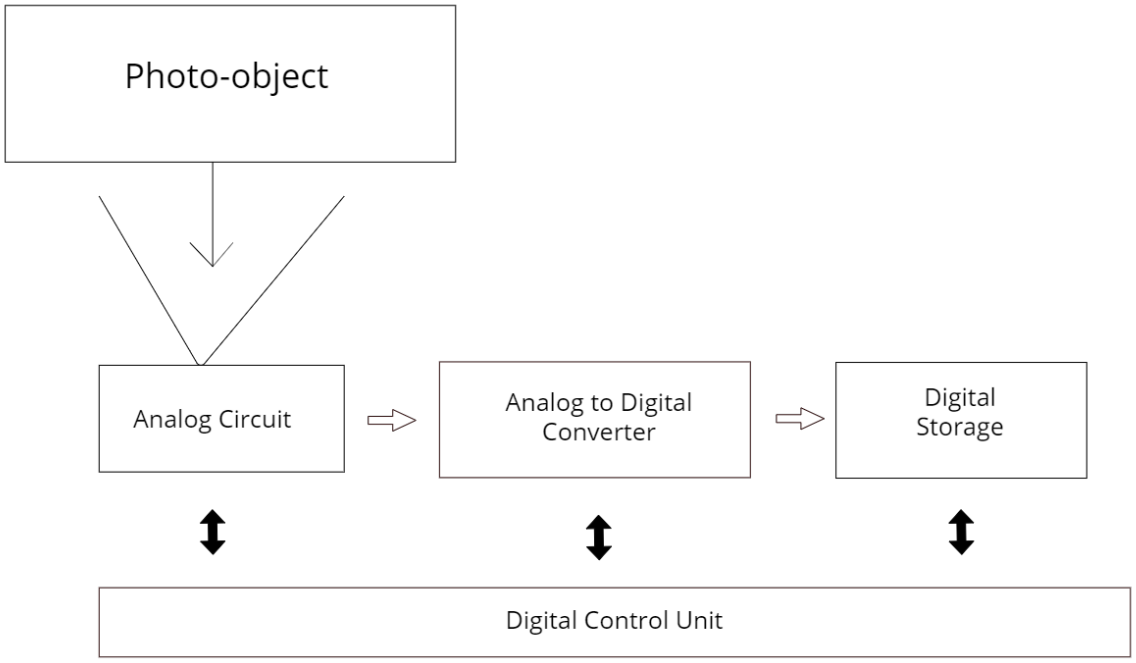


Figure 1: An overview of the system flow inside the digital camera to be designed.

In Figure 2 a block diagram for the readout circuit and control unit is shown. With the exception of the **Clk** signal, which is the internal clock of the camera and the **Reset** signal, all the input signals are available to the user. The **Reset** signal is used to reset (the meaning of this will be defined in subsection 3.3) the camera. All processes will be aborted should it be set `HIGH` while a photograph is being captured and digitalised. The **Increase_time** and **Decrease_time** are used to increase and decrease, respectively, the exposure time the camera will use when capturing the photograph. The digital control unit, denoted RE_Control in Figure 2, governs the **NRE_1**, **NRE_2**, **ADC**, **Expose** and **Erase** signals which are used as input signals to the analog circuit associated with each pixel inside Pixel_electronics. When the **Init** signal is set `HIGH` (`HIGH` and `LOW` will be used throughout this text to represent logic high and low respectively) by the user, the photo capturing process is initiated. The

implementation of the pulse shaper will be taken for granted and will not be discussed. When each pixel has been exposed to light for a user determined time, the values stored in the analog circuit in Pixel_electronics are converted from analog to digital values. When this process is done the control unit tells the camera to stand by and wait for the initiation of the next photograph.

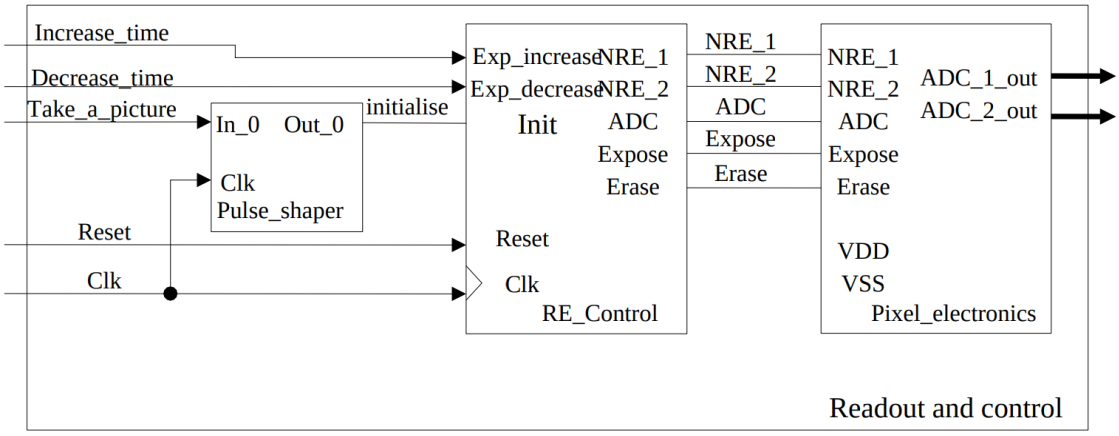


Figure 2: Block diagram for the readout circuit and control unit. [2]

## 2.1 Analog readout circuit

Figure 3 shows the circuit topology for the analog circuit inside Pixel_electronics. For the purposes of this design process a photodiode and current generator represents the input photo detector. Bright light will be simulated with a strong current and dim light will be simulated with a weak current. All transistor are assumed to be of the enhancement type. The current from the photodiode leads to charging of the capacitor, $C_S$ which in turn sets up a voltage potential over $C_S$, $V_{C_S}$. Note that the $V_{C_S}$ voltage is the same as the source voltage of the M1 transistor. However current can only flow into the capacitor under the assumption that the **Expose** signal is `HIGH`, allowing current to flow through the transistor and charging the capacitor. When **Expose** is `LOW` the M1 transistor will not conduct any current from the drain terminal to the source terminal (with the exception of leakage current, to be discussed in subsection 3.1). The charge stored in $C_S$ and thus the voltage value across it, will remain unaffected.

The M2 transistor in parallel with $C_S$ controls the erasing of the charge stored in $C_S$. Whenever the **Erase** is `LOW` the transistor acts as an open circuit and has no impact on the circuit. However, when the **Erase** is set to `HIGH` the source terminal will be connected to ground. This will short-circuit $C_S$, discharging it and making the voltage across it zero.

It is evident that the M1 transistor controls when each pixel should be exposed to light and the M2 transistor is tasked with controlling when the value stored in each pixel should be erased. It is clear that they have conflicting roles and that their control signals should not be `HIGH` simultaneously. When designing the digital control unit the **Erase** signal will be given priority.

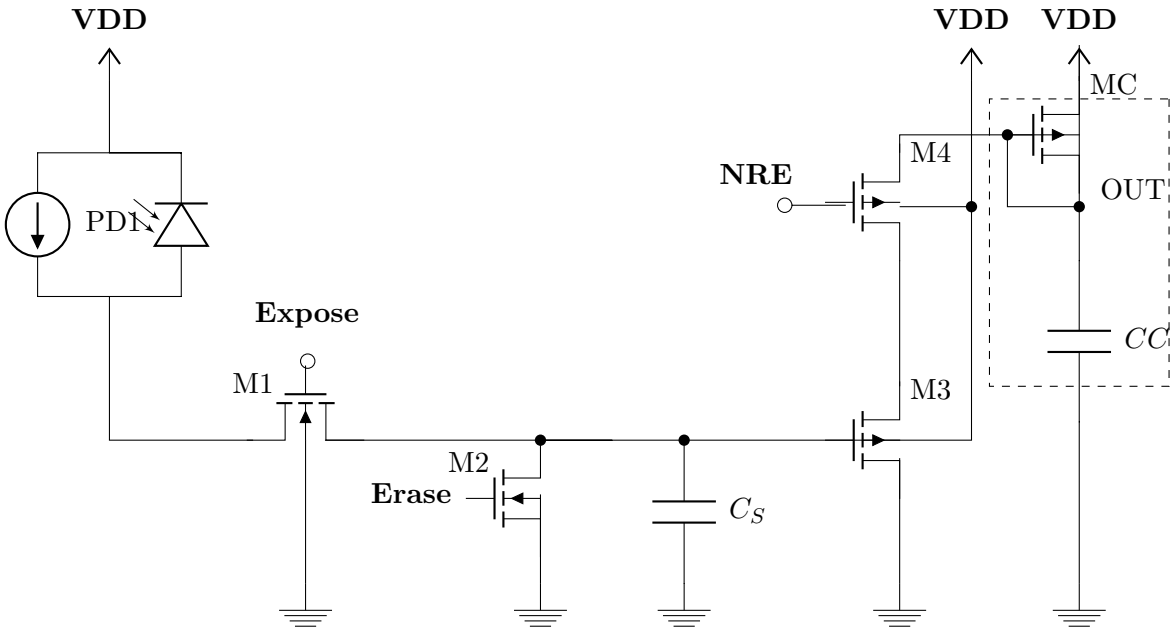


Figure 3: Pixel circuit

Before the discussion of the remaining transistors of the circuit, the composition of the four pixels that make up the Pixel_electronics will be introduced and briefly discussed to ensure the understanding of the analog circuit. The pixel composition is shown in Figure 4. The four pixel modules, Pixel 1_1, Pixel 1_2, Pixel 2_1 and Pixel 2_2 each contains the pixel circuit shown in Figure 3. The pixels are arranged in a grid pattern, where the pixels in the same row share a **NRE** signal (i.e Pixel 1_1 and Pixel 1_2 share the NRE_1 signal) and pixels in the same column share the same ADC (i.e Pixel 1_1 and Pixel 2_1 share ADC_C1) and MC and CC transistor-capacitor pair (i.e Pixel 1_1 and Pixel 2_1 share the MC1 transistor and CC1 capacitor). Note that the MC transistor and CC capacitor encircled by a dashed line in Figure 3 is shared between two pixels in the same column. From the pixel structure in Figure 4 it is clear that only pixels in the same row can be converted simultaneously. Therefore the **NRE_1** and **NRE_2** should not be set `LOW` at the same time. This will be kept in mind when discussing the digital control unit.

Proceeding with the discussion of the circuit in Figure 3 with the pixel composition in Figure 4 kept in mind, it is clear that the M3 and MC transistors of Figure 3 act as a buffer between the capacitor voltage, $V_{C_S}$ and the output terminal connected to ADC. The buffer transistor, M3, uses the MC transistor as an active load. The purpose of this buffer is to avoid any impact on the $V_{CS}$ voltage by the OUT terminal. The M3 and MC transistors are connected by the M4 transistor. The M4 transistor is in turn controlled by the **NRE** signal and similarly to the M1 and M2 transistor it operates as a voltage controlled switch. However, as it is a PMOS transistor it can only conduct current when the gate **NRE** signal is `LOW`. When this is the case the switch is closed and current can conduct from the source terminal to the drain terminal. This actives the readout of the charge stored in the $C_S$ capacitor. The buffer circuit transfers the capacitor voltage, ideally with a gain of 1 (a discussion of gain follows in subsection 3.1) not impacting the voltage value, from the M3 gate to the OUT terminal. Thus the voltage value of $V_{CS}$ is loaded at input of the ADC and is ready to be

converted.

## 2.2 Digital control unit

A block diagram of the digital control unit, RE_control is shown in Figure 5. In addition to the **Clk** and **Reset** signal, it takes as its input the signals **Init**, **Exp_increase** and **Exp_decrease** all available to the user as mentioned in section 2. RE_control will output the signals **NRE_1**, **NRE_2**, **Expose**, **Erase** and **ADC** all of which are used as input signals to the pixel circuit in Pixel_electronics as discussed in section 2. In addition to the input and output signals, there exists three internal signals, **Ovf5**, **Start** and **EX_time**. These are used for internal communication between the submodules CLTR_ex_time, Timer_counter and FSM_ex_ctrl whose behaviour are to be discussed.

The CTRL_ex_time submodule stores the amount of clock cycles the exposure process are to use. Whenever the **Reset** signal is set `HIGH` a default exposure time value is loaded. If the user desires, he or she could increase or decrease this amount of clock cycles by setting the **Exp_increase** or **Exp_decrease** `HIGH` respectively. The exposure time will be increased with as many clock cycles as the increase or decrease signals are `HIGH`. Thus, if i.e the **Exp_increase** signal is `HIGH` during 4 clock signals, the exposure time increases with 4 clock cycles. However the user cannot increase the exposure time forever, and consequently there exists an upper and lower constraint on the exposure time value.

The Timer_control submodule is tasked with counting the amount if clock cycles the exposure process is to last for. When the **Start** signal is toggled from `LOW` to `HIGH` it counts the amount of clock cycles given by the signal **EX_time**. The counter overflows when the counting of pre-set clock cycles are done which sets the **Ovf5** signal `HIGH`, indicating to the FSM_ex_control submodule that the exposure time has finished.

The module FSM_ex_control controls the submodules CTRL_ex_time and Timer_counter as well as all output signals and can be considered the brain of the photo capturing operation. When the user triggers the **Init** signal it passes through a pulse shaper (as mentioned in the discussion of Figure 2) making sure that it is only `HIGH` during one clock cycle. This tells the FSM_ex_control to initiate the capturing of a photograph. This involves changing the **Erase** signal from `HIGH` to `LOW` and the **Expose** from `LOW` to `HIGH` as well as setting the **Start** signal during one clock cycle. Subsequently the EX_time value given by CTRL_ex_time is loaded into the Timer_counter module which in turn counts the amount of clock cycles given by EX_time. When the counting is done, Timer_counter sets the **Ovf5** signal `HIGH` indicating to the FSM_ex_control that the exposure process has finished. Exposure is thus set `LOW` as no more exposure is wanted and the image has been captured. FSM_ex_control then initiates the process of reading and converting the values stored in the capacitor in each pixel module.

As mentioned when discussing the behaviour of the analog circuit in subsection 2.1 only a pair of two pixel may have their values converted by the two ADCs simultaneously. Consequently the output signals NRE_1 and NRE_2 may not be toggled concurrently. Since the NRE_1 and NRE_2 signals are used to toggle a PMOS switch they should be set `LOW` when a value is to be converted and set to `HIGH` otherwise. During the first clock cycle of the readout process one of the switching signals i.e NRE_1 has to be set `LOW` so that the capacitor voltage is loaded at the terminals of the ADC in accordance with Figure 3 and Figure 4. During the subsequent cycle the ADC signal is set `HIGH` and the voltage values for the pixel pair loaded in the previous cycle are converted to the corresponding digital values. Then during the next

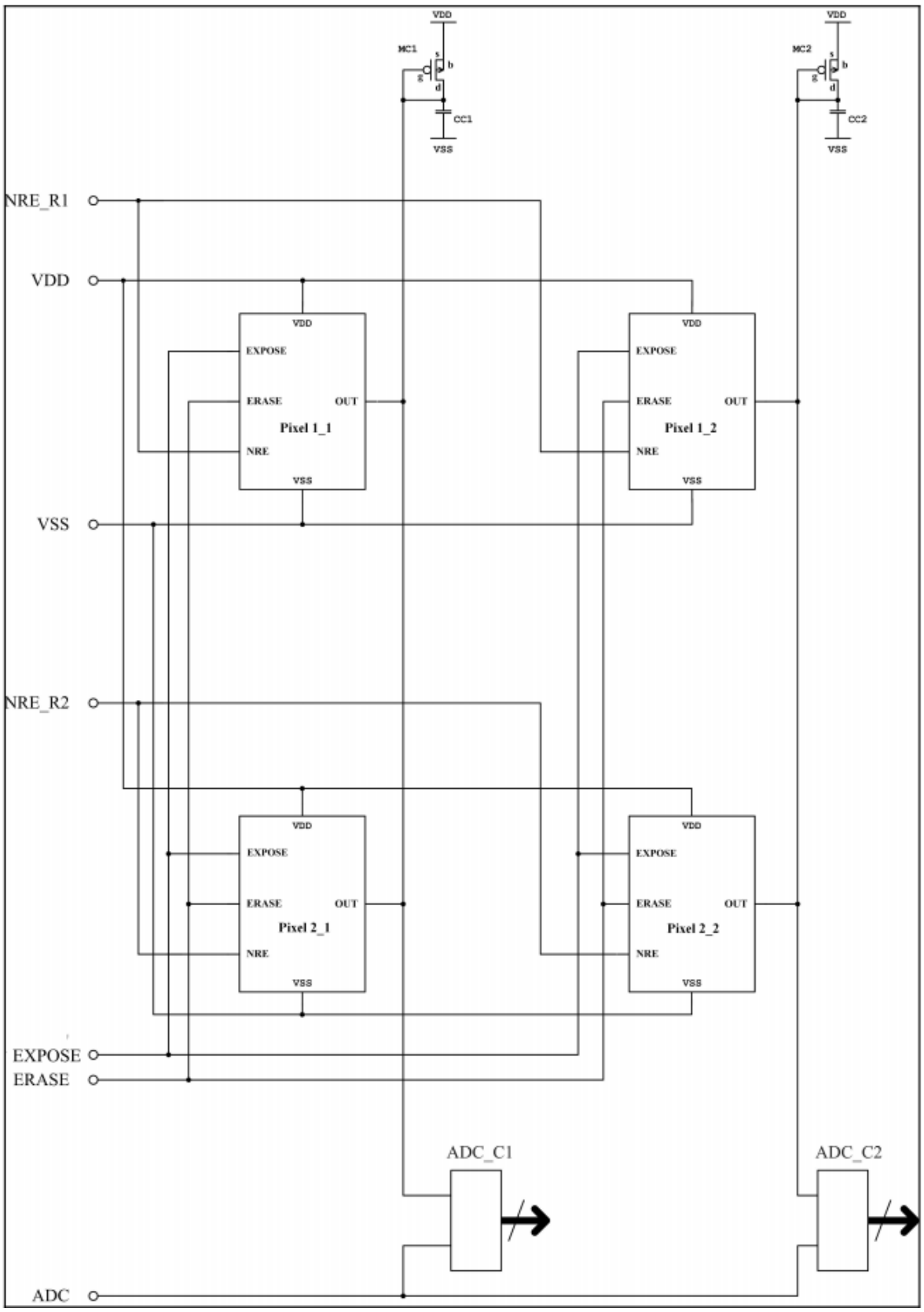


Figure 4: Block diagram of the pixel array [2]

cycle, ADC is set `LOW` again and during the next cycle, which is the fifth one of the readout stage, the NRE_1 is set `HIGH`. The process is then repeated for the NRE_2 signal. During the sixth cycle **NRE_2** is set `LOW` so that the pair of pixels connected to the **NRE_2** signal can be converted. As is in the case of the NRE_1 signal, ADC is set `HIGH` for one cycle while the values are being converted. Once the values are converted ADC is set `LOW` again and in the final clock cycle NRE_2 gets toggled back to `HIGH`. Thus the readout process lasts for a total of 9 clock cycles. For a clearer overview the values of each output signal of RE_control during the readout process is summarised in Table 1.

Once finished with the readout process, the erase signal is set `HIGH`, erasing the values in the capacitors inside each of the pixels. The FSM_ex_control then waits for the initiating of the next photograph in which the aforementioned process is repeated. Note that unless the user changes the exposure time in between the capturing of two photographs (or the **Reset** signal is set `HIGH`), it will remain unchanged.

Table 1: Values of output signals when reading analog values into the digital converter.

| **Clock Cycle** | **NRE_1** | **NRE_2** | **ADC** | **Expose** | **Erase** |
|---|---|---|---|---|---|
| #1 | 1 | 1 | 0 | 0 | 0 |
| #2 | 0 | 1 | 0 | 0 | 0 |
| #3 | 0 | 1 | 1 | 0 | 0 |
| #4 | 0 | 1 | 0 | 0 | 0 |
| #5 | 1 | 1 | 0 | 0 | 0 |
| #6 | 1 | 0 | 0 | 0 | 0 |
| #7 | 1 | 0 | 1 | 0 | 0 |
| #8 | 1 | 0 | 0 | 0 | 0 |
| #9 | 1 | 1 | 0 | 0 | 0 |

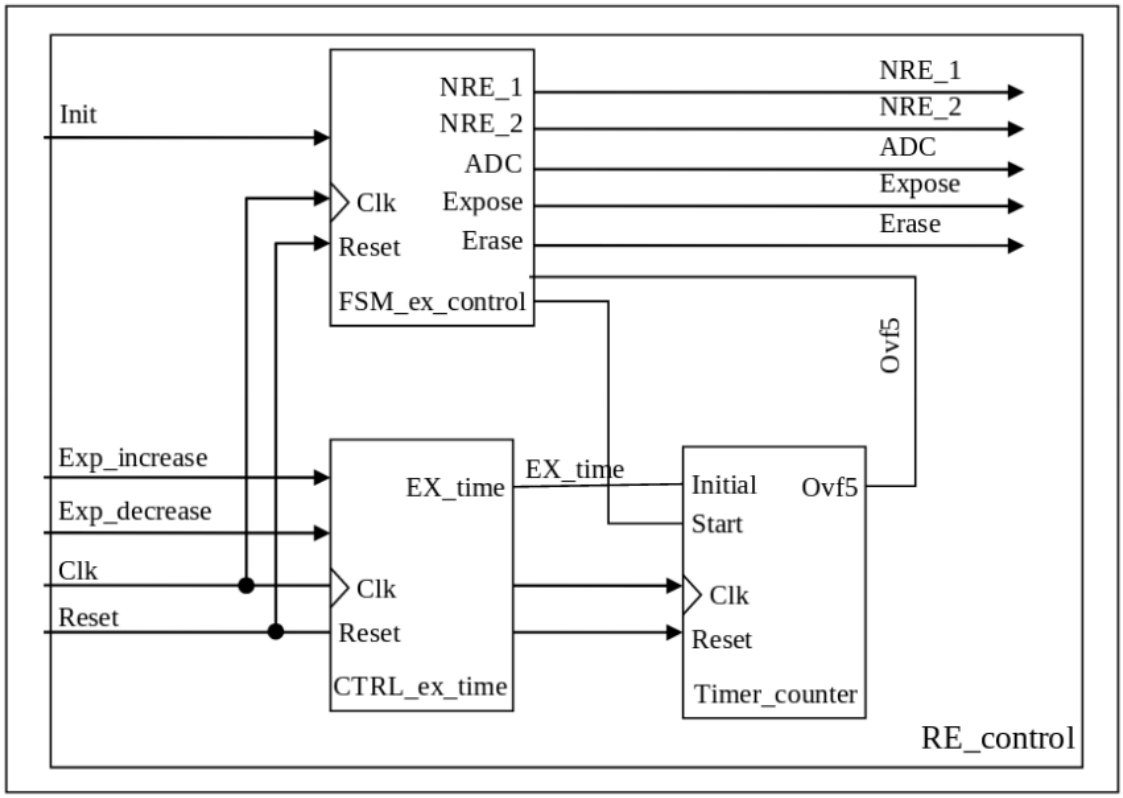


Figure 5: Block diagram of the digital control unit [2]

# 3 Design

## 3.1 Analog design

With the topology of the pixel circuit given as described in subsection 2.1 the problem of designing the analog part of the camera reduces to determining the parameter sizes of the components in the circuit. In specific terms, the width and length of the transistor gate has to be determined within a given range of $W_{min} < W < W_{max}$ and $L_{min} < L < L_{max}$ specified as a requirement of the implementation of the circuit. Similarly the capacitance of $C_S$ also has to determined to a value lower then a specific value, $C_S < C_{S_{max}}$ also given as a requirement when implementing the camera. The value of the $CC$ capacitor is given and is not in need of determination [2].

It is evident from the circuit topology in Figure 3 and the discussion of its behaviour in subsection 2.1 that the M1 and M2 transistors both behave as switches. When the gate to source voltage, $V_{GS,M1}$, is higher than the threshold voltage of the transistor, $V_T$, the switch the transistor is modelling is closed and allows the conduction of current,$I_D$, from drain to source. When $V_G = 0$ the gate source voltage is lower than the threshold voltage (this is under the assumption that the capacitance of $C_S$ is such that $V_S < V_T$ no matter the amount of charge stored in the transistor).

Assuming the body-effect to be negligible (the justification of such an assumption will be discussed in subsection 3.2), consider the approximation of the drain current in the sub-

threshold region in a NMOS transistor given by (1)

$$I_{D(sub-th)} \approx I_{D0}(\frac{W}{L})e^{\frac{qV_{eff}}{nkT}} \tag{1}$$

where $I_{D0}$, $q$ and $nkT$ are predetermined transistor characteristics and $V_{eff}$ is the gate-source to threshold voltage difference; $V_{eff} = V_{GS} - V_T$ [1]. When the gate voltage is zero the sub-threshold drain current given by (1) becomes

$$\begin{aligned} I_{D(off)} &\approx I_{D0}(\frac{W}{L})e^{\frac{q(-V_S - V_T)}{nkT}} \\ &\approx \lambda(\frac{W}{L})e^{-qV_S} \end{aligned} \tag{2}$$

where

$$\lambda = I_{D0}e^{\frac{-qV_T}{nkT}} \tag{3}$$

From (2) it is evident that it exists a $V_S$-dependent drain current, $I_{D(off)}$ albeit $V_{GS}$ being lower than the threshold value. In other words; despite the exposure signal being off, a "leakage current" can flow into the capacitor, affect the voltage over the capacitor and consequently a distortion of the digitally stored photograph could occur. As such an outcome is undesirable the aforementioned leakage current should be minimised. From (2) it is clear that by making the gate- width to length ratio, $\frac{W}{L}$, as small as possible within the given constrains the effects from the leakage current will be minimised.

Similarly, in the case of the one of the two other switch-acting transistors, M2 the effects of leakage current could cause serious harm to the camera. The M2 transistor controls the erasing of charge in the $C_S$ capacitor. If a considerable amount of current is allowed to flow from drain to source when transistor is meant to be off, it would short-circuit the capacitor and information about the picture would be lost. Therefore, in an effort to minimise the described effects of leakage current, the gate- width to length ratio, $\frac{W}{L}$, should be minimised within the boundaries given on the M1 and M2 transistors.

The problem of determining the gate with and length of the M3 and MC transistor depends on the desired behaviour of the buffer circuit. When discussing the behaviour of the circuit in subsection 2.1 it was mentioned that ideally the buffer has a gain equal to 1. Technically, as no information is given about the range of values the ADC can convert, whether the gain is equal to one or larger is irrelevant. This follows from the fact that, assuming the ADC can convert all values, whether the actual value of $V_{CS}$ or an amplified value of i.e $2 \cdot V_{CS}$ is stored in the memory location is irrelevant as it is simply a matter of re-programming what value should correspond to a given colour brightness. However, the gain of the buffer is not irrelevant. It is desirable that the difference between the maximum capacitor voltage $V_{CSmax}$ and the minimum capacitor voltage, $V_{CSmin}$, is kept within a certain range.

If the camera were to be implemented with a real ADC, this ADC would have a specific range and the extent to which it is able to distinguish between values would depend on its quantization precision. Consequently, should the voltage range of the capacitor be to narrow, the precision of the ADC might not be sufficient to store the voltage values with the required accuracy. If the gain of the buffer is considerably lower than 1, i.e 0.3, the voltage range would shrink proportionally and the voltage range could be too low for the ADC as discussed. It can be shown that the maximum theoretical gain of the buffer circuit in Figure 3 is equal to

1. Hence, the transistor should be dimensioned in an attempt to make the gain of the buffer as close to 1 as possible in order to keep the voltage range of the capacitor as high as possible.

When the **NRE** signal goes `LOW` to initiate the readout, the M4 transistor will be in the active region. However the MC transistor is initially in the subthreshold region as the capacitor $CC$ is charged so that $V_{GS} < V_{th}$ at the initiation of the readout. When readout is activated, the capacitor is quickly discharged and MC enters the active region. This results in a buffer with an unstable gain until the MC transistor operates in the active area. However, as previously discussed the **NRE** signal goes `LOW` one clock cycle before the voltage value is to be converted by the ADC. It is only important that the circuit is stable when the voltage is to be read by the ADC. Therefore, if one clock cycle lasts for a considerable amount of time compared to the time the MC transistor needs to be in the active region this momentary (relative to the clock period) instability can be ignored.

Considering the transistors when they are in the active region, the drain current through a PMOS transistor, $I_D$, is given by the square-law relationship [1] in (4).

$$\begin{aligned} \mathrm{I_D} &= \frac{\mu_\mathrm{n}\mathrm{C_{ox}}}{2}\frac{\mathrm{W}}{\mathrm{L}}\left(-V_\mathrm{eff}\right)^2 \\ &= \beta\frac{W}{L}(V_{eff})^2 \end{aligned} \tag{4}$$

where $V_\mathrm{eff} = V_{GS} - V_{tn}$ is the same as in (1) and $\beta = \frac{\mu_\mathrm{n}\mathrm{C_{ox}}}{2}$ is a predetermined transistor characteristic. Note that since the M3 and MC transistors are of PMOS type, a minus sign has to be included in front of $V_{eff}$ in (4). However as this value is squared, it is removed for simplicity in the next line. By studying the pixel circuit in Figure 3 it is clear that the $V_\mathrm{eff}$ values for the M3 and MC transistors are given by (5) and (6) respectively.

$$V_{\mathrm{eff},M3} = V_{out} - V_{in} - V_{tn} \tag{5}$$

$$V_{\mathrm{eff},M3} = V_{DD} - V_{out} - V_{tn} \tag{6}$$

$V_{DD}$, $V_{out}$ and $V_{in}$ are the supply voltage, output voltage that the ADC reads and input voltage to the buffer circuit ($V_{in} = V_{CS}$) respectively. The ADC is assumed to have an infinite input impedance and consequently the current through the M3 and MC transistors must be the same. With equal drain current, from (4), (5) and (6) the following relationship between the transistor parameters is obtained

$$\begin{aligned} \beta_3\frac{W_3}{L_3}(V_{out} - V_{in} - V_{tn})^2 &= \beta_C\frac{W_C}{L_C}(V_{DD} - V_{out} - V_{tn})^2 \\ \frac{W_3}{L_3}(V_{out} - V_{in} - V_{tn})^2 &= \frac{W_C}{L_C}(V_{DD} - V_{out} - V_{tn})^2 \end{aligned} \tag{7}$$

where the $\beta$ values cancel each other as they are the same for each transistor. When the transistors are operating in the active area the $V_{eff}$ values are positive. Thus the following inequalities are satisfied

$$\begin{aligned} V_{out} - V_{in} &\geq V_{tn} \\ V_{DD} - V_{out} &\geq V_{tn} \end{aligned} \tag{8}$$

Squaring (7) gives

$$k_3 \left(V_{out} - V_{in} - V_{tn}\right) = k_C \left(V_{DD} - V_{out} - V_{tn}\right) \tag{9}$$

where $k_3 = \sqrt{\frac{W_3}{L_3}}$ and $k_C = \sqrt{\frac{W_C}{L_C}}$. Solving (9) with respect to $V_{out}$ yields

$$V_{out} = \frac{k_3}{k_3 + k_C} V_{in} + \frac{k_C}{k_3 + k_C} V_{DD} + \frac{k_3 - k_C}{k_3 + k_C} V_{tn} \tag{10}$$

To maximise the gain of the buffer it is clear from (10) that $k_3$ should be as high as possible and $k_C$ as low as possible within the given constrains. This corresponds to $W_3 = W_{max}$ and $L_3 = L_{min}$ in addition to $W_C = W_{min}$ and $L_C = L_{max}$.

In the case of M4, it is clear from Figure 3 that it acts like a switch. It controls the initiation of the readout process for its corresponding pixel. As mentioned in subsection 3.1 only one pair of pixels should be read simultaneously. Thus, if a considerable leakage current exists in the M4 transistor two pixel pairs could be read simultaneously, and consequently the ADC would digitise a combination of two pixels creating an erroneous image. Although M4 is a PMOS transistor (1) and (2) holds if the signs of all voltages are swapped. By re-evaluating (2) with swapped voltage signs, it is clear that the magnitude of the leakage current still is proportional to the $\frac{W}{L}$ ratio.

However, the M4 transistor is also part of the buffer circuit and therefore its impact on the buffer circuit must be considered. When in the active region the drain current through the M4 transistor is also given by the square-law relationship in (4). From (4) it is clear that by minimising the $\frac{W}{L}$ ratio, less drain current will conduct. If this is the case the M4 transistor will effectively act as a resistor in the buffer circuit. Should this resistance be significant it will impact the buffer circuit and decrease the accuracy of the model in which the M3 and MC parameters were determined. Thus the choice comes down to minimising the impact on the buffer circuit at the cost of a higher leakage current or vice versa. However, since the pixel circuit has a low output impedance while in readout (which is the process under consideration) it will not be significantly affected by the weak leakage current from another pixel output. Therefore it is desirable to minimise the impact M4 has on the rest of the buffer circuit, and $\frac{W}{L}$ should be set as high as possible within the given constraints.

It is clear that the maximum input voltage to the buffer, $V_{in_{max}} = V_{CS_{max}}$ has to be one that satisfies the inequalities given by (8) as it is required to ensure that the transistor operates in the active region. By considering (10) with a given value for $V_{DD}$ and $V_{tn}$ the maximum value that satisfies (8) can be found. Similarly the minimum input voltage that ensures the transistor operating in the active region can be found. With these values, denoted $V_{CS_{max}}$ and $V_{CS_{min}}$ kept in mind, the capacitance of the $C_S$ capacitor can be determined. The voltage across a the $C_S$ capacitor is given by (11)

$$V_{CS} = \frac{1}{C_S} \int_0^{t_0} I(\tau) \mathrm{d}\tau \tag{11}$$

Since the current source simulating the light is assumed to be DC, the current is constant and the integral in (11) evaluates to

$$V_{CS} = \frac{I \cdot t_0}{C_S} \tag{12}$$

Solving (12) with respect to $C_S$ yields

$$C_S = \frac{I \cdot t_0}{V_{CS}} \tag{13}$$

By evaluating (13) in the extreme case of maximum current from the current source during the minimum exposure time with the maximum allowed voltage over the capacitor, a minimum value, $C_{S_{min}}$ can be found. Since an upper constraint is given as a specification requirement to the camera, picking a $C_S$ value in the range $C_{S_{min}} < C_S < C_{S_{max}}$ will suffice.

### 3.2 A discussion of body effect

The discussion and usage of the equations modelling the transistor behaviour in the preceding subsections are based on the assumption that bulk terminal is connected to the source terminal resulting in an voltage difference from source to bulk, $V_{SB}$, equal to zero. However as can be seen in Figure 3 this is not the case for the M1, M3 and M4 transistors. In the case of these transistors, the bulk and source terminals are disconnected resulting in $V_{SB} > 0$ (as the bulk is grounded for the NMOS transistors and the bulk is at $V_{DD}$ for the PMOS transistor). Consequently the amount of charge and conduction through the transistor will be influenced by the $V_{SB}$ voltage.

This *body effect* is modelled as an increase in the threshold voltage, $V_{tn}$, in the transistor. By including the body effect the moderated threshold voltage is given by (14)

$$\mathrm{V_{tn}} = \mathrm{V_{tn0}} + \gamma(\sqrt{\mathrm{V_{SB}} + |2\phi_\mathrm{F}|} - \sqrt{|2\phi_\mathrm{F}|}) \tag{14}$$

where $\Phi_F$, $\gamma$ and $C_{ox}$ are the Fermi potential of the bulk, the body effect constant and gate capacitance per unit area, given by (15), (16) and (17) respectively.

$$\Phi_F = \frac{kT}{q} \ln(\frac{N_A}{n_i}) \tag{15}$$

$$\gamma = \frac{\sqrt{2\mathrm{qN_A K_s}\varepsilon_0}}{\mathrm{C_{ox}}} \tag{16}$$

$$C_\mathrm{ox} = \frac{\mathrm{K_{ox}}\varepsilon_0}{\mathrm{t_{ox}}} \tag{17}$$

As the equations (15), (16) and (17) introduces a considerable amount of new parameters their physcial meaning is best described by a table. Table 2 summarises the psychical meaning and sizes of the parameters introduced in (15), (16) and (17). Out of the parameters presented in Table 2 the thickness of the thin oxide under the gate, $t_{ox}$, the acceptor concentration, $N_A$, are parameters that are unique for the transistor. These values are specified in the files used when modelling the transistor during the software run tests.

With the values from Table 2 inserted in (15), (16) and (17) the body effect constant is computed to be $\gamma \approx 2.29{\cdot}10^{-7}\sqrt{\mathrm{V}}$ and the Fermi potential is computed to $\Phi_F \approx 0.533\mathrm{V}$. When implementing the circuit the supply voltage and the transistors used will give a $V_{SB}$ voltage with a magnitude around 1V. Evaluating (3.2) with these values inserted, yields a modified threshold voltage of $V_{tn} \approx 0.45000012\mathrm{V}$, an increase of $1.2 \cdot 10^{-7}\mathrm{V}$. As this corresponds to a relative increase of 0.00002666666% the neglecting of the body effect is justified.

Table 2: Values of constants introduced.

| | | |
|---|---|---|
| $\epsilon_0$ | $8.8\times10^{-12}$ $\mathrm{Fm}^{-1}$ | Vacuum permittivity |
| $\mathrm{K}_{ox}$ | 3.9 $\mathrm{Fm}^{-2}$ | Relative permittivity of SiO2 |
| $\mathrm{t}_{ox}$ | $\frac{4.1}{0.95} \times 10^{-9}$m | Thickness of the thin oxide under the gate |
| q | $1.6 \times 10^{-19}$C | Elementary charge |
| $\mathrm{K}_S$ | 11.8 | Relative permittivity of Silicon |
| $\mathrm{n}_i$ | $1.1 \times 10^{16}$ | Carrier concentration of intristic silicon |
| $\mathrm{n}_a$ | $10^{11}$ | Acceptor concentration |

### 3.3 Digital Design

As the discussed behaviour of the camera can be divided into three states, one idle state awaiting the initiating of the photograph, one exposure state exposing each pixel to light and a readout state where values are converted from analog to digital, it is suitable to implement the digital control unit, RE_control, by using a Finite State Machine (FSM). A flowchart of the machine to be designed is shown in Figure 6.

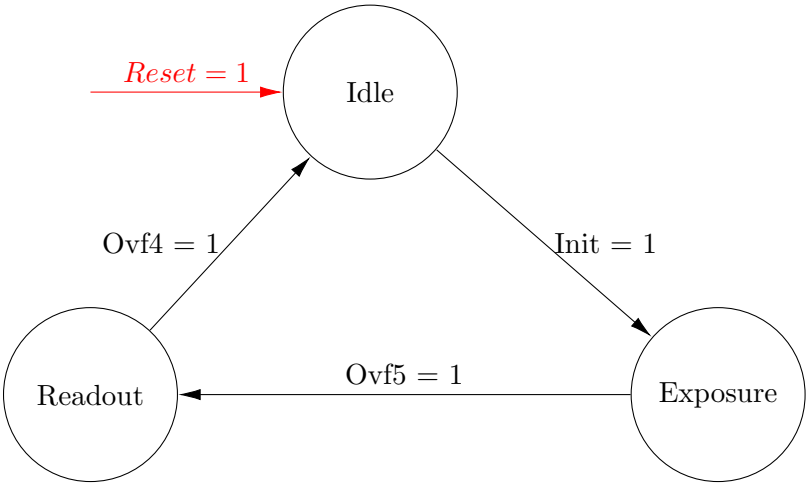


Figure 6: State diagram of the Finite State Machine to be designed. The red "Reset" arrow indicates a prioritised state jump should it be set to high.

Each state is identified by a unique set of output signals. In the Idle state, the camera is simply waiting for the initiation of the next capturing process, in the Exposure state the camera exposes the pixels to the light and in the Readout state the values obtained from the exposure state is converted. The output signals that identify each state, is set in accordance with the discussion in subsection 2.2. They are presented in Table 3. The output values of the Readout state have been omitted from this table both for viewing purposes and as they are presented in Table 1 and thoroughly discussed insubsection 2.2.

As is clear from the state diagram in Figure 6 in each state there is only one possible next state to jump to which is controlled by only one signal for each state, excluding the triggering of **Reset**. While in the Idle state, the only possible next state is the Exposure state. The transition to this state occurs when the **Init** signal is set `HIGH` by the user. In the Exposure sate the output signals are set as listed in Table 3. As discussed in subsection 2.2

a counter counts the amount of clock cycles the exposure state should lasts. This counter overflows when the counting is done, setting the **Ovf5** signal **HIGH** for once clock cycle. The **Ovf5** signal being set `HIGH` is what triggers the jump from Exposure to the only possible next sate, Readout. In the readout state the output signals changes with the timings presented in Table 1. Recall that the Readout state requires 9 clock cycles to complete the readout.

An additional counter inside the FSM starts counting when the machine transitions from the Exposure state to the Readout state. Once this counter has counted the 9 clock cycles required in the Readout state it overflows, similarly to the counter in the exposure state, and sets the **Ovf4** signal `HIGH` during one clock cycle. The toggling of the **Ovf4** signal is the only signal the can trigger the jump from the Readout state to the Idle state. Once back in the Idle state, the output signals are set in accordance with Table 3 it remains in this state until the user triggers the **Init** signal, restarting the process. The entire photo capturing process is illustrated with a timing chart for all the signals involved with the FSM shown in Figure 7.

The red arrow pointing at the Idle state in Figure 6, indicates that whenever the **Reset** signal is set `HIGH`, the machine should jump to the Idle state no matter what other state the machine may be in. If the camera were to be realised, a mechanism ensuring that the **Reset** signal is set `HIGH` when the camera powers up should be installed. This ensures that the camera is always in the Idle state to begin with. It also loads the default exposure time into the CTRL_ex_time module. An important difference between the Idle state triggered by the **Ovf4** and the Idle state triggered by the **Reset** signal is that the **Reset** signal resets the exposure time stored in the submodule CTRL_ex_time discussed in subsection 2.2 to its default value, the **Ovf4**-triggered jump doesn't. Unless the user takes action, the exposure time will remain the same as in the previous picture.

Table 3: The values of all output signals for each state in the state machine. For the values of **NRE_1**, **NRE_2** and **ADC** during readout, see Table 1

| **State** | **NRE_1** | **NRE_2** | **ADC** | **Erase** | **Expose** |
|---|---|---|---|---|---|
| Idle | 1 | 1 | 0 | 1 | 0 |
| Exposure | 1 | 1 | 0 | 0 | 1 |
| Readout | - | - | - | 0 | 0 |

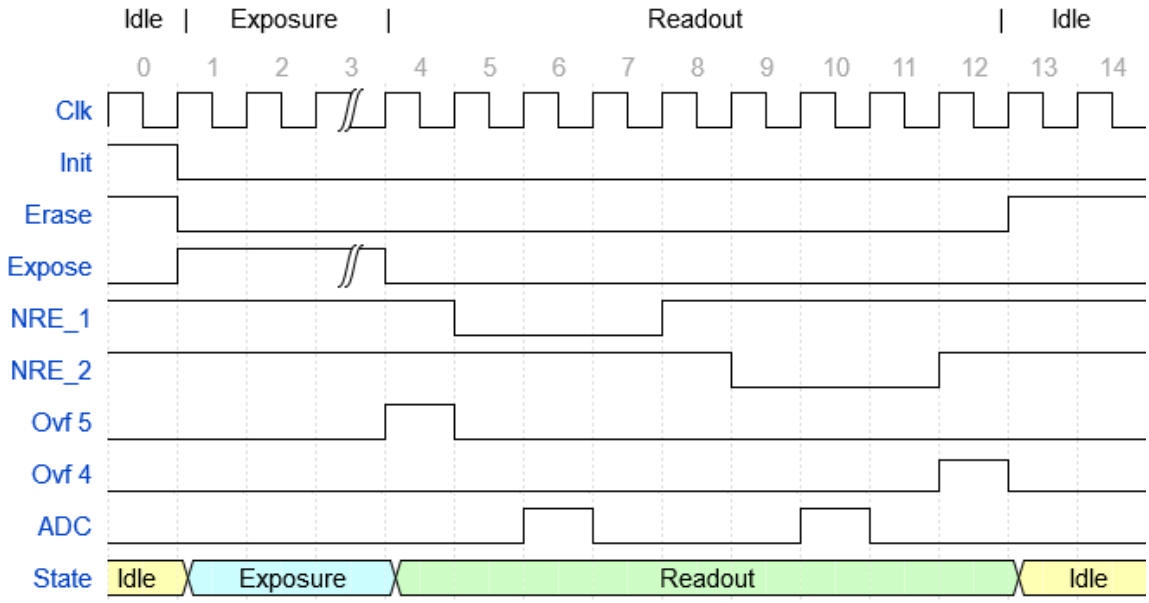


Figure 7: Timing chart for the signals in the FSM. Note that curved lines on the **Expose** and **Clk** signal indicates that this state could last for a longer or shorter time.

# 4 Implementation and testing

The implementation of the analog circuit and digital control unit was done based upon a set of pre-determined requirements on the components. These requirements are summarised in Table 4. The analog circuit implemented uses 180nm transistor technology with a threshold voltage $V_{tn} = 0.45$. The gate width and length of each transistor is decided in accordance with the requirements in Table 4 and the discussion in subsection 3.1. The values of each transistor is listed in Table 5. With these transistor values, a supply voltage of $V_{DD} = 1.8$V and a threshold voltage of $V_{tn} = 0.45$V the maximum and minimum voltage over the capacitor $C_S$ are found to be $V_{CS_{max}} = 0.9$V and $V_{CS_{min}} = 0$V from (8) and (10). Evaluating (13) with this maximum voltage as well as the maximum current and minimum exposure time given by Table 4 yields a minimum capacitance of 1.67pF. Therefore $C_S$ is selected to be 2pF which satisfies both the lower and upper constraint.

With a supply voltage og $V_{DD} = 1.8$V the potential difference between the source and bulk on all transistors will have a magnitude of around $1V$, which justifies the neglecting of the body effect as discussed in subsection 3.2. Furthermore, a clock frequency of 1kHz equals a clock period of 1ms. This is a considerable longer amount of time than the MC transistor spends in the subtreshold region (which is a matter of picoseconds). Therefore the circuit is stable long before the subsequent clock cycle when the ADC is set to read the values as discussed in subsection 3.1. A clock period of 1 ms and a desired exposure time given in the millisecond range means that the counters in the digital control unit can count the desired exposure times by counting clock cycles, as discussed in subsection 2.2.

Table 4: The system requirements of the camera to be implemented.

| **Parameter** | **Value** |
|---|---|
| $V_{DD}$ | 1.8V |
| Clock frequency | 1kHz |
| Max gate width | 5.040$\mu$m |
| Min gate widht | 1.08$\mu$m |
| Max gate length | 1.08$\mu$m |
| Min gate length | 0.36$\mu$m |
| Max $C_S$ capacitance | 3pF |
| $CC$ | 3pF |
| Max exposure time | 30ms |
| Min exposure time | 2ms |
| Maximum photo current | 750pA |
| Minimum photo current | 50pA |

Table 5: The values used when implementing the analog circuit.

| **Parameter** | **Value** |
|---|---|
| $W_{M1}$ | 1.08$\mu$m |
| $W_{M2}$ | 1.08$\mu$m |
| $W_{M3}$ | 5.05$\mu$m |
| $W_{M4}$ | 5.05$\mu$m |
| $W_{MC}$ | 1.08$\mu$m |
| $L_{M1}$ | 1.08$\mu$m |
| $L_{M2}$ | 1.08$\mu$m |
| $L_{M3}$ | 0.36$\mu$m |
| $L_{M4}$ | 0.36$\mu$m |
| $L_{MC}$ | 1.08$\mu$m |
| $C_S$ | 2pF |

## 4.1 Testing of analog circuit

To test the analog circuit it was implemented and simulated using the analog circuit simulating software AIM-Spice. The AIM-Spice code produced is included in Appendix B. The anaolog cirucit has been tested with the two extreme cases of maximum exposure time with minimum current and minimum exposure time and maximum current.

The result of the two simulations are shown in Figure 8 and Figure 9. As can be be seen from the figures, the capacitor reaches almost the same voltage values in both cases as is to be expected. Also notice that the maximum voltage the capacitor reaches is almost 0.9V which is what was expected from theory.

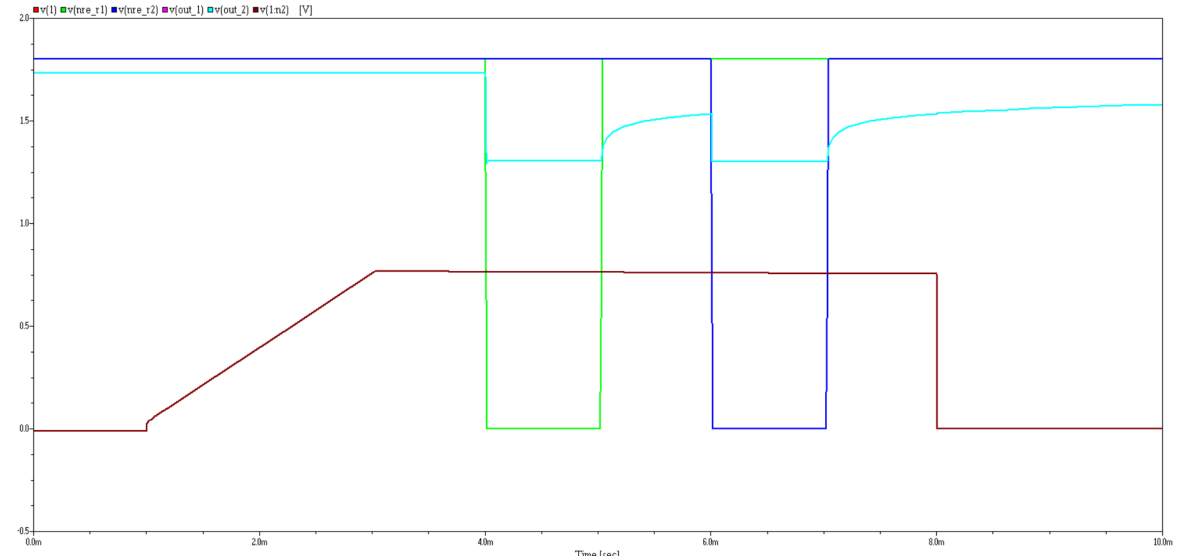


Figure 8: Testing the analog circuit with 2ms exposure time and a 750pA current. Brown is $C_S$ capacitor voltage. Light blue is the output voltage the ADC reads. Darker blue and green are the **NRE_2** and **NRE_1** signals respectively.

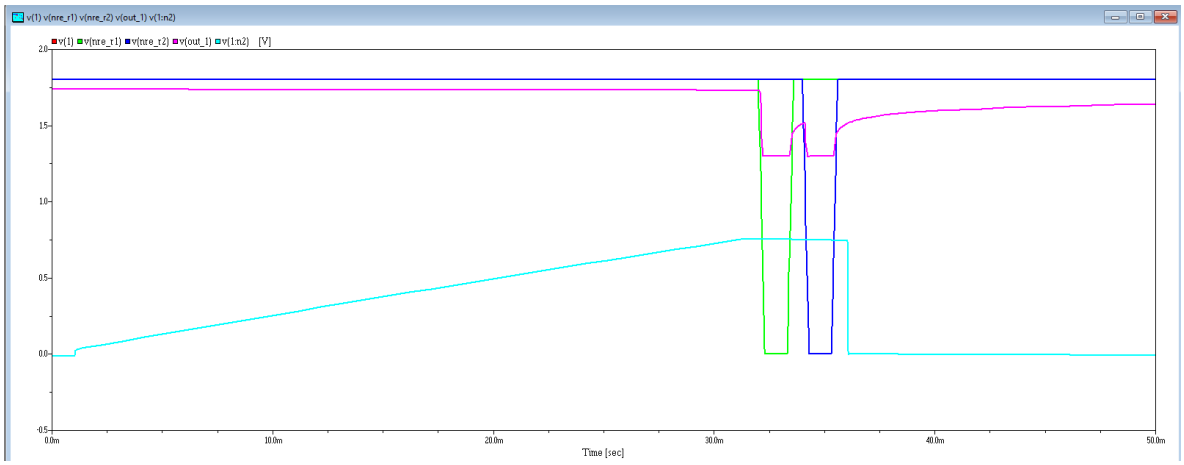


Figure 9: Testing the analog circuit with 30ms exposure time and a 50pA current. Light blue is $C_S$ capacitor voltage. Pink is the output voltage the ADC reads. Darker blue and green are the **NRE_2** and **NRE_1** signals respectively.

## 4.2 Testing of digital control unit

To test the digital control unit the Finite State machine discussed in subsection 3.3 was implemented using the hardware description language Verilog. The FPGA design, creation and simulation software Active HDL was used to run simulations on the written code to test its functionality. When implementing the CTRL_ex_time module a default exposure time of 14 clock cycles was chosen. The Verilog Source code produced is included in Appendix A. Three different test have been done to ensure the functionality of the finite state machine.

A simulation with the goal of testing the most basic functionality, the capturing of one photograph, has been run. The resulting timing diagram is shown in Figure 10. As can be seen seen in Figure 10, the **Exp_increase** signal is `HIGH` for a total of 4 clock cycles. When the camera enters the Exposure state it lasts for a total of (14+4) cycles which is the desired amount of time. The timing of the output signals during readout happens as discussed in subsection 2.2. In total, the test gave the same timing diagram as the desired one shown in Figure 7.

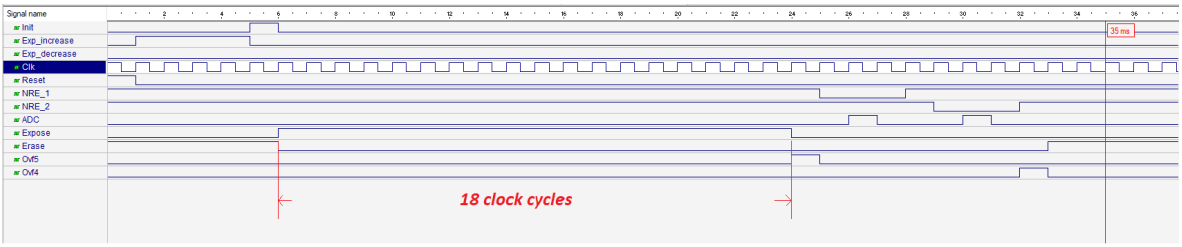


Figure 10: Timechart of a simulation were one picture has been taken.

To ensure that the exposure time value remains unaffected while in idle state a test where two pictures were taken subsequently without the reset signal getting triggered in between has been done. The resulting timing diagram is shown in Figure 11. The results of this test clearly shows that finite state machine can capture subsequent photographs. The exposure time is the same for both capturing processes and the signals in the readout state also have their desired behaviour.

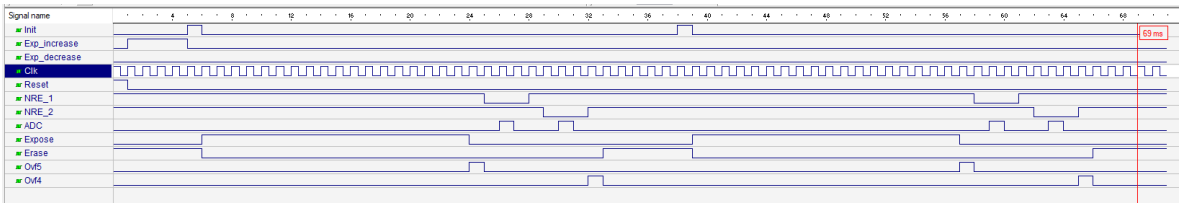


Figure 11: Timechart of a simulation were two subsequent pictures are taken.

The last test conducted is done to ensure that the **Reset** signal works as discussed. A simulation where the **Reset** signal goes `HIGH` in while in the exposure state has been done. The time diagram is shown in Figure 12. As it shows, the **Reset** signal works as intended. The **Expose** signal goes `LOW` and the **Erase** signal goes `HIGH` once the **Reset** signal is triggered. In hindsight to fully test the functionality of the **Reset** signal, a the initiation of a new photograph should have been done in this simulation to verify if the exposure time is reset to its default value.

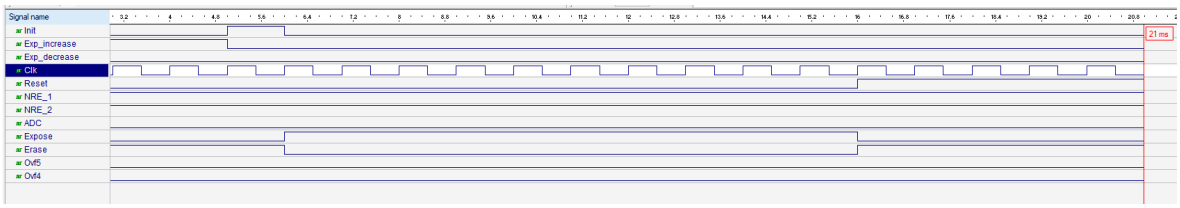


Figure 12: Timechart of a simulation were the Reset signal is triggerd.

As shown in Figure 10, Figure 11 and Figure 12 the testing of the finite state machine gives the desired output signals as discussed in theory.

# 5 Conclusion

A the design of the analog sampling circuit and the digital control unit in a digital have been discussed. The analog circuit have been implemented and simulated using AIM-Spice while the digital control unit has been implemented and simulatied using the hardware description language Verilog with the aid of Active HDL for simulations. The determination of paramters have been done in accordance with a set of given system requirements. After verifying the digital control unit in Active HDL the circuit using Aimspice, it can be concluded that the design process have been sucsessfull.

In the current implementation, exposure time needs to be held down for the amount of clock-cycles to be adjusted. If a physical camera is to be realised a button mechanism where CTRL_ex_time reacts on rising Exp_increase and Exp_increase should be realised for better functionality. If the camera is only intended for usage by a computer such a mechanic is not needed.

# 6 References

## References

[1] Tony Chan Carusone, David Johns and Kenneth Martin. *Analog integrated circuit design international student edition.* John Wiley & sons Singapore Pte. Ltd, 2013

[2] Bjørn B Larsen. *TFE4152 – Design of integrated circuits 2019, Project description, Digital camera*

# Appendices

## A Verilog source code

### A.1 CTRL_ex_time.v

```
1  // CTRL_ex_time
2  /*  The task of this module is to store the exposure time
3      aswell as letting the user increment and decrement the
4      value of the exposure time
5  */
6
7  // Using 1ms since we are operating and incrementing at the
       milisecond range
8  // 1 ns should be enough for precision. If the rounding is off by 1
        ns it shouldn't
9  // matter since we are operating at the 1ms scale.
10 `timescale 1ms / 1ns
11
12 // Output is a 4 bit number representing the amount of unit
       exposure.
13 // Since the timescale definition sets 1ms = 1 unit, the 4 bit
       number represents
14 // exposure time in units.
15 module CTRL_ex_time(input wire exp_increase, exp_decrease, Clk,
       Reset,
16     output reg [4:0]  EX_time);
17         always @ (posedge Clk)
18             begin
19                 //  If the reset button is pressed the default
                       should be held
20                 // Since reset is assumed to be high at power up,
                       EX_time will always be
21                 // assigned a value
22                 if (Reset == 1'b1)
23                     EX_time <= 5'd14;
24                 else if (exp_increase == 1'b1 && EX_time < 5'b11110
                       )
25                     EX_time <= EX_time + 1;
26                 else if (exp_decrease == 1'b1 && EX_time > 5'b10)
27                     EX_time <= EX_time - 1;
28             end
29 endmodule
```

### A.2 Timer_counter.v

```
1  // Timer counter
2  // The task of this module is to count initial amounts of time
       cycles
3  // It will set the ovf5 flag high when it is done counting.
4
5  // Using 1ms since we are operating and incrementing at the
       milisecond range
6  // 1 ns should be enough for precision. If the rounding is off by 1
        ns it shouldn't
7  // matter since we are operating at the 1ms scale.
8  `timescale 1ms / 1ns
9
10 module Timer_counter (input wire Clk, Reset,
11     input wire [4:0] Initial,
12         input wire Start,
13     output reg Ovf5);
14
15     reg [4:0] cycle_counter;
16     logic done_counting;
17
18         always @ (posedge Clk, posedge Reset)
19             begin
20                 if (Reset) begin
21                     cycle_counter <= 0;
22                     Ovf5 <= 0;
23                     done_counting <= 0;
24                     end
25                 // We should only count while reset is low
26                 // We also need start to be high to initiate the
                       counting
27                 // This requires start to be high throughout the
                       counting
28                 else if (Reset == 0 && Start == 1)
29                     cycle_counter <= cycle_counter + 1;
30                 else if (Reset == 1'b0 && cycle_counter > 0 &&
                       cycle_counter != Initial)
31                     cycle_counter <= cycle_counter + 1;
32                 else if (cycle_counter == Initial) begin
33                     Ovf5 <= 1'b1;
34                     cycle_counter <= 1'b0;
35                     done_counting <= 1;
36                 end
37                 if (done_counting) begin
38                     Ovf5 <= 0;
39                     done_counting <= 0;
```

```
40                  end
41
42                  // If reset is high, the counting should be stopped
43                  // Cycle counter should be set to zero to prepare
                        for next countdown
44                  // Ovf5 should be set low
45
46
47              end
48  endmodule
```

### A.3 fsm.v

```
1
2  // FSM_ex_control
3  module FSM_ex_control (input wire Init, Clk, Reset, Ovf5,
4      output reg NRE_1, NRE_2, ADC, Expose, Erase, Start,
5      output logic Ovf4);
6
7      // Ovf4 signal is included as an output for plotting purposes.
8      // Technically this is an internal signal of the FSM and should
9      // be declared inside the module
10
11     // Defining states
12     parameter [1:0] Idle = 2'b00;
13     parameter [1:0] Exposure = 2'b01;
14     parameter [1:0] Readout = 2'b10;
15
16     reg [1:0] current_state, next_state;
17     reg [4:0] counter;
18
19     always @ (posedge Clk) begin
20         if (Reset == 1'b1 || Ovf4) begin
21             current_state <= Idle;
22             counter <= 5'b00000;
23             Ovf4 <= 0;
24             end
25         // If we are in readout, we should start counting
26         else if (current_state == Readout && counter < 9) begin
27                 counter <= counter + 1;
28                 current_state <= next_state;
29             end
30         else
31             current_state <= next_state;
32     end
33
34         always @ (*)
35         begin
36             next_state <= current_state; //Default is not to move
37
38             // Set default signals. This corresponds to idle state.
39             NRE_1 <= 1;
40             NRE_2 <= 1;
41             Erase <= 1;
42             Expose <= 0;
43             ADC <= 0;
44             Start <= 0;
```

```
45
46
47              case (current_state)
48                  Idle : begin
49                      // To prepare for the eventual readout state.
50                      Ovf4 <= 0;
51                      counter <= 5'b00000;
52
53                      // No need to change signals in this state.
54                      // They are assigned by default
55                          if (Init == 1 && Reset == 0) begin
56                              next_state <= Exposure;
57                              Erase <= 1;
58                              Start <= 1;
59                              Expose <= 0;
60                          end
61                          else
62                              next_state <= current_state;
63                              end
64
65                  Exposure : begin
66                          // Change necessary signals
67                          Erase <= 0;
68                          Expose <= 1;
69                          Start <= 0;
70
71                          if (Reset == 1)
72                              next_state <= Idle; // Reset has
                                    priority
73                          else if (Reset == 0 && Ovf5 == 1) begin

74                              // This corresponds to the first cycle
                                    in the readout stage
75                              Expose <= 0;
76                              next_state <= Readout;

77
78                              end
79                          else if (Reset == 0 && Ovf5 == 0) begin
80                              next_state <= current_state;
81                              Expose <= 1;
82                              end
83                      end
84                  Readout : begin
85                      // Erase, Expose and Start are all LOW during
                            Readout
86                      // Setting values for the second readout stage
```

```
87                      // These values will be set if the counter is
                           zero
88
89                       Expose <= 0; Erase <= 0; Start <= 0;
90                       NRE_1 <= 0; NRE_2 <= 1; ADC = 0;

91                       Ovf4 <= 0;

92
93                       //Change signals depending on how far in
                            readout we are

94                       if (Reset)
95                           // Reset has priority
96                           next_state <= Idle;
97
98                           else if (counter == 1) begin

99                               NRE_1 <= 0; NRE_2 <= 1; ADC <= 1;
                                       // 3
100                          end
101                          else if (counter == 2) begin

102                              NRE_1 <= 0; NRE_2 <= 1; ADC <= 0;
                                       // 4
103                          end
104                          else if (counter == 3) begin
105                              NRE_1 <= 1; NRE_2 <= 1; ADC <= 0;
                                       // 5
106                          end
107                          else if (counter == 4) begin

108                              NRE_1 <= 1; NRE_2 <= 0; ADC <= 0;
                                       // 6


109                          end
110                          else if (counter == 5) begin

111                              NRE_1 <= 1; NRE_2 <= 0; ADC <= 1;
                                    // 7
112                          end
113                          else if (counter == 6) begin

114                              NRE_1 <= 1; NRE_2 <= 0; ADC <= 0;
                                    // 8
115                          end
```

```
116                                 else if (counter == 7) begin

117                                     NRE_1 <= 1; NRE_2 <= 1; ADC <= 0;
                                            // 9
118                                     // Readout is done
119                                     // Reset of Ovf4 is taken care of
                                            in the first always statement (
                                            in line 19)
120                                     Ovf4 <= 1;
121                                     next_state <= Idle;
122                                 end
123
124
125
126                             end
127
128                 default : next_state <= current_state;
129             // 0
130     endcase
131     end
132 endmodule
```

### A.4 re_control.v

```
1  // RE_control
2  module RE_control (input reg Init, Exp_increase, Exp_decrease, Clk,
       Reset,
3      output wire NRE_1, NRE_2, ADC, Expose, Erase,
4      output logic Ovf5, Ovf4);
5
6      logic Start;
7      logic [4:0] EX_time;
8
9      //FSM
10     FSM_ex_control FSM (Init, Clk, Reset, Ovf5, NRE_1, NRE_2, ADC,
           Expose, Erase, Start, Ovf4);
11
12     //Timer Counter
13     Timer_counter TC (Clk, Reset, EX_time, Start, Ovf5);
14
15     //Control EX_Time
16     CTRL_ex_time CTRL_EX(Exp_increase, Exp_decrease, Clk, Reset,
           EX_time);
17
18
19 endmodule
```

# B Aimspice source code

## B.1 pixel_til_rapport.cir

```
1  IC prosjekt
2
3  .include p18_cmos_models.inc ! Transistor model from BB
4  .include p18_model_card.inc  ! Transistor model from BB
5
6  * Testbench from BB
7  * ---------------------------------
8  .param Ipd_1 = 750p ! Photodiode current, range [50 pA, 750 pA]
9  .param VDD = 1.8 ! Supply voltage
10 .param EXPOSURETIME = 2m ! Exposure time, range [2 ms, 30 ms]
11
12 .param TRF = {EXPOSURETIME/100} ! Risetime and falltime of EXPOSURE
       and ERASE signals
13 .param PW = {EXPOSURETIME} ! Pulsewidth of EXPOSURE and ERASE
      signals
14 .param PERIOD = {EXPOSURETIME*10} ! Period for testbench sources
15 .param FS = 1k; ! Sampling clock frequency
16 .param CLK_PERIOD = {1/FS} ! Sampling clock period
17 .param EXPOSE_DLY = {CLK_PERIOD} ! Delay for EXPOSE signal
18 .param NRE_R1_DLY = {2*CLK_PERIOD + EXPOSURETIME} ! Delay for
      NRE_R1 signal
19 .param NRE_R2_DLY = {4*CLK_PERIOD + EXPOSURETIME} ! Delay for
      NRE_R2 signal
20 .param ERASE_DLY = {6*CLK_PERIOD + EXPOSURETIME} ! Delay for ERASE
       signal
21
22 VDD 1 0 dc VDD
23 VEXPOSE EXPOSE 0 dc 0 pulse(0 VDD EXPOSE_DLY TRF TRF EXPOSURETIME
      PERIOD)
24 VERASE ERASE 0 dc 0 pulse(0 VDD ERASE_DLY TRF TRF CLK_PERIOD PERIOD
      )
25 VNRE_R1 NRE_R1 0 dc 0 pulse(VDD 0 NRE_R1_DLY TRF TRF CLK_PERIOD
      PERIOD)
26 VNRE_R2 NRE_R2 0 dc 0  pulse(VDD 0 NRE_R2_DLY TRF TRF CLK_PERIOD
      PERIOD)
27
28 .plot V(OUT1) V(OUT2) ! signals going to ADC
29 .plot V(EXPOSE) V(NRE_R1) V(NRE_R2) V(ERASE)
30 .plot V(OUT_SAMPLED1)
31
32 * Component parameters
33 *-------------------------
34 .param C_s=2p
```

```
35 .param L_M1= 1.08u
36 .param L_M2=1.08u
37 .param L_M3= 0.36u
38 .param L_M4= 0.36u
39
40 .param W_M1=1.08u
41 .param W_M2=1.08u
42 .param W_M3=5.05u
43 .param W_M4=5.05u
44
45 .param L_MC1=1.08u
46 .param W_MC1=1.08u
47 .param C_c1= 3p
48
49 .param L_MC2=1.08u
50 .param W_MC2=1.08u
51 .param C_c2=3p
52
53 * Main Circuit (Pixel Grid)
54 *-------------------------------------------------
55 MC1 OUT_1 OUT_1 1 1 PMOS L=L_MC1 W=W_MC1
56 CC1 OUT_1 0 C_c1
57 MC2 OUT_2 OUT_2 1 1 PMOS L=L_MC2 W=W_MC2
58 CC2 OUT_2 0 C_c2
59
60 X1 EXPOSE ERASE NRE_R1 OUT_1 1 0 PixelCircuit
61 X2 EXPOSE ERASE NRE_R1 OUT_2 1 0 PixelCircuit
62 X3 EXPOSE ERASE NRE_R2 OUT_1 1 0 PixelCircuit
63 X4 EXPOSE ERASE NRE_R2 OUT_2 1 0 PixelCircuit
64
65
66 * Pixel Circuit
67 * ------------------------------------------------
68 .subckt PixelCircuit EXPOSE ERASE NRE OUT VDD VSS
69 X5 VDD N1 PhotoDiode
70 M1 N1 EXPOSE N2 VSS NMOS L=L_M1 W=W_M1
71 M2 N2 ERASE VSS VSS NMOS L=L_M2 W=W_M2
72 M3 VSS N2 N3 VDD PMOS L=L_M3 W=W_M3
73 M4 N3 NRE OUT VDD PMOS L=L_M4 W=W_M4
74 CS N2 VSS C_s
75 .ends
76
77 * Photo diode handed out on BB
78 * ---------------------------------------
79 .subckt PhotoDiode VDD N1_R1C1
80 I1_R1C1 VDD N1_R1C1 DC Ipd_1
81 d1 N1_R1C1 vdd dwell 1
```

```
82 .model dwell d cj0=1e-14 is=1e-12 m=0.5 bv=40
83 Cd1 N1_R1C1 VDD 30f
84 .ends
```